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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,636	10/10/2003	Nadeem N. Eleyan	004-30059	1191

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,636	ELEYAN ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-40* is/are allowed.

6)☒ Claim(s) *1-3,8,13,15,24,25,41 and 42* is/are rejected.

7)☒ Claim(s) *4-7,9-12,14 and 16-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 02/16/2006 has been entered.

2. Claims 1-22, 24-42 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-22,24-42 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. Regarding claim 22, the content in dependent claim 22 is disclosed in independent claim 16.

Claim should be canceled or amended.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 41-42 are rejected under 35 U.S.C. 102(b) as being anticipated by El Hajji (U.S. Patent No. 6,038,187).

Regarding claims 41-42, El Hajji discloses an apparatus (Column 8, lines 58-67, Column 9, lines 1-10) comprising:

means for detecting in situ (Column 1, lines 60-63, Column 8, lines 15-17) a sensing offset in a sensing circuit that includes a cross-coupled pair transistors (Column 8, lines 58-65, *sense/restore amplifier comprises two inverters, and each inverter is formed by two complementary transistors*) , and means for characterizing a magnitude of sensing offset (Column 1, lines 42-49), and means for characterizing a direction of sensing offset (Column 9, lines 1-7).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-3,8,13,15,24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurth et al. (Pub. U.S. Patent No. 2004/0008534).

Regarding claim 1, Kurth et al. disclose a test block (Figure 4, 211) for memory circuit (Figure 1), wherein the test block is configures to characterize in situ a sensing offset (ABSTRACT) of a sensing circuit including a cross-coupled pair of transistors (Figure 4, 210, 212, [0038], *pair of cross-coupled Q1, Q2*).

Regarding claim 2, Kurth et al. disclose wherein the test block selectively introduces discharge paths into respective halves of a differential circuit sensed by the sensing circuit [0041, *the conduction of n-channel transistor causes the low-voltage digitline to be discharge toward the NLAT* voltage*).

Regarding claim 3, Kurth et al. disclose wherein the discharge paths are selectively introduces to characterize a direction of the sensing offset (ABSTRACT, *sense amplifier circuitry can be offset in one embodiment to defaut to be the un-programmed state*, [0042], *unprogrammed*, [0051]).

Regarding claim 8, Kurth et al. disclose an integrated circuit (Figure 4) comprising:

a first and second plurality of control signals (Figure 4, ACT, EPSA*, RNL*(B), RNL*(A);

a first and second plurality of ports (Figure 4, 227A, 227B); and

at least a first and second discharge path (Figure 4, NLAT1, NLAT2) coupled to at least one of the respective first and second plurality ports ([0041]) , the effective strengths of the first and second discharge paths determined by respective ones of the first and second plurality of control signals (0041], *ACT 270*), the first and second discharge paths configurable for characterization of sensing offset associated with sensing circuit ([0041-0042], *the sense amplifier circuitry is biased to sense the unprogrammed ROM cells as a logic one data state*).

Regarding claim 13, Kurth et al. disclose wherein the first and the second plurality of control signals selectively enable at least one of a first plurality of transistors

(Figure 4, 219) and at least one of a second plurality of transistors coupled to respective ones of the first and the second of plurality of ports (Figure 4, 208A, 208B).

Regarding claim 15, Kurth et al. disclose a first and second opposing bitline (Figure 4, 202A, 202B) selectively coupled to the first and the second discharge paths.

Regarding claim 24, Kurth et al. disclose embodied in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit ([0025]).

Regarding claim 25, Kurth et al. disclose embodied in cache of a processor integrated circuit ([0025]).

Allowable Subject Matter

8. Claims 4-7,9-12, 14,16-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-7, 9-12,14,16-22 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kurth et al. (Pub. U.S. Patent No. 2004/0008534), El Hajji (U.S. Patent No. 6,038,187), and others, does not teach the claimed invention having wherein the discharge paths are selectively introduced to characterize a magnitude of sensing offset as claim 4 disclosed, and wherein the sensing offset results, at least in part, from an accumulated data- dependent mismatch in characteristics of the cross-coupled transistors as claim 5 disclosed, and wherein the sensing offset results, at least in part, from a disparate, negative bias temperature

instability induced shift in threshold voltage (Vt) of at least one of the cross-coupled transistors based on disparate voltage bias histories thereof as claim 6 disclosed, and wherein the sensing offset results, at least in part, from process variations in either the transistors or differential pair circuits to which the transistors are coupled as claim 7 disclosed, and wherein the first and the second discharge paths are selectively loaded to vary the strengths of the first and the second discharge paths as claim 0 disclosed, and wherein the first and the second discharge paths are selectively enabled, the first and the second discharge paths selected from respective ones of a first and a second plurality of discharge paths of varying strengths as claim 10 disclosed, and wherein the first and the second plurality of control signals selectively couple at least respective ones of a first and a second capacitive load to the respective ones of the first and the second plurality of ports as claim 11 disclosed, and wherein the first and the second plurality of control signals selectively couple at least a first and a second resistive load to the respective ones of the first and the second plurality of ports as claim 12 disclosed, and wherein the first and the second plurality of control signals selectively enable at least one of a first plurality of inverters and at least one of a second plurality of inverters coupled to respective ones of the first and the second plurality of ports as claim 14 disclosed, and a control block for generating the first and second plurality of control signals based at least in part on detection of a sensing offset of a sensing circuit including a cross-coupled pair of transistors as claims 16-22 disclosed.

Claims 26-40 are allowed.

Claims 26-40 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kurth et al. (Pub. U.S. Patent No. 2004/0008534), El Hajji (U.S. Patent No. 6,038,187), and others, does not teach the claimed invention having a method of detecting in situ a sensing offset in a sensing circuit including a pair of cross-coupled transistors comprises an introducing the pair of discharge paths into respective halves of differential circuit and sensing the differential circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

Thoyle